REMARKS

Applicants hereby traverse the outstanding rejection, and request reconsideration and withdrawal in light of the remarks contained herein. Claims 1-24 are pending in this application.

Rejection under 35 U.S.C. §103(a)

Claims 1-21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ho, U.S. Patent No. 6,128,768 (hereinafter "*Ho*"), in view of Mahajan, U.S. Patent No. 6,327,696 (Hereinafter "*Mahajan*").

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. See M.P.E.P. §2143. Without conceding the second and third criteria, Applicants assert that the rejection does not satisfy the first criteria.

It is well settled that the proposed modification cannot render the prior art unsatisfactory for its intended purpose, M.P.E.P. §2143.01. If the proposed modification rendered the prior art unsatisfactory for its intended purpose, then there is no valid suggestion or motivation to make the proposed modification. *Ho* teaches a method of extracting layout parasitics for nets of an integrated circuit using a connectivity-based approach. The Examiner concedes that *Ho* does not teach VLSI design in register transfer language (RTL), but states that it would have been obvious to change *Ho* to use RTL because it is mentioned in *Mahajan*.

Without conceding that *Ho* teaches VLSI design, it is not possible to use register transfer language in *Ho*, because *Ho* teaches a layout extraction method, see abstract. Attempting to use register transfer language with a layout extraction method would render that method inoperable. Layout extraction techniques require defined layouts, which have the necessary libraries of chip architecture, chip geometry, and chip geography. In fact, the use of "a lookup library of defined geometries" is a fundamental aspect of *Ho*'s method, see *Ho*

column 3 lines 19-25. Chip layouts, such as those of *Ho*, are typically expressed in GDS2 type languages, which support the requisite libraries. The register transfer language the Examiner proposes as a modification to *Ho* does not have the ability to support libraries of specific chip architecture, chip geometry, and chip geography. Because a system and method that requires these libraries can not use a language format incapable of supporting them, *Ho* can not use register transfer language and still function for its intended purpose. Thus the Examiner's rejection of the claims 1-21 as obvious in view of the *Mahajan*'s use of RTL is improper.

No valid suggestion has been made as to why a combination of *Ho* and *Mahajan* is desirable. Therefore, the rejection of claims 1-21 should be withdrawn.

New claims 22-24 depend directly from base claims 1, 11, and 21, respectively, and thus inherit all limitations of their respective base claims. Each of claims 22-24 sets forth features and limitations not recited by the combination of *Ho* and *Mahajan*. Thus, the Applicants respectfully assert that new claims 22-24 should be indicated as being allowable over the art of record.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made"**.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Please see the enclosed authorization to charge fee due to our Deposit Account No. 08-2025, under Order No. 10001834-1 from which the undersigned is authorized to draw.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV256037355US in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date shown below.

Date of Deposit: February 17, 2003

Typed Name: John Pallivathukal

Signature: _____

Respectfully submitted,

By _____
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Date: February 17, 2003

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Version With Markings to Show Changes Made

New claims 22, 23, and 24 have been added as follows:

22. (New) A method according to claim 1 wherein the said estimating signal routes between functional blocks occurs prior to the final determination of a layout.

23. (New) A VLSI chip according to claim 11 whose design was performed according to the method wherein said estimating signal routes between functional blocks occurs prior to the final determination of a layout.

24. (New) A system according to claim 21 wherein said estimating signal routes between functional blocks occurs prior to the final determination of a layout.